Self-Heating Effects in Gate-all-around Silicon Nanowire MOSFETs: Modeling and Analysis

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Abstract

In this paper, an electro-thermal model is proposed for the first time to accurately investigate the self-heating effects in gate-all-around (GAA) silicon nanowire MOSFETs (SNWTs) for thermal-aware design optimization. The model is derived based on the equivalent thermal network method, in which the impacts of gate length dependence, nanowire diameter dependence and surface roughness on the nanowire channel thermal conductivity as well as the influence of unique GAA structure features on the heat dissipation are taken into account. The proposed model agrees well with the experimental results of SNWTs. Based on the model, the impacts of structure parameters on the current driving capabilities and heat dissipation of SNWTs are discussed. The developed electro-thermal model can be further applied to the thermal-aware design of SNWT-based circuits.

Keywords

Gate-all-around (GAA), silicon nanowire MOSFET (SNWT), self-heating effect, equivalent thermal network.

1. Introduction

The gate-all-around (GAA) silicon nanowire MOSFET (SNWT) has shown great potential to be one of the promising candidates for future nanotechnology, due to their excellent electrostatics, superior transport and CMOS compatibility [1-5]. However, severe self-heating in SNWTs leads to the degradation of device performance and reliability problems because of the confined device geometry and increased phonon boundary scattering. Our previous experimental results show that the self-heating effect of GAA SNWTs even built on fully-Si bulk substrate (FSB) with SiO_2 gate dielectric is comparable to that of planar SOI devices [6] and it is also reported that GAA SNWTs with high-k/metal gate stack still exhibits non-negligible self-heating effects [7].

To simulate self-heating effects, modeling equivalent thermal network is an efficient way, because it takes into account the structural features and can be easily embedded into both device and circuit-level simulations [8-11]. However, such model and analysis of self-heating effects in SNWTs have not been reported. In modeling equivalent thermal network of SNWTs, a scalable compact model of thermal conductivity of silicon nanowire channel is an important part. It is reported that the thermal conductivity of silicon nanowires is determined by critical structure parameters, such as channel length, nanowire diameter and surface roughness of silicon nanowires [12-19]. Thus this intrinsic part should be accurately modeled and considered in practical analysis of self-heating effects in SNWTs.

In this paper, we propose an electro-thermal model by developing the equivalent thermal network of GAA SNWTs on fully-Si bulk substrate. Unique features of GAA structure and the structure dependent thermal conductivity of silicon nanowire channels are considered. This model can be also easily extended to GAA SNWTs based on SOI substrate. Based on the electro-thermal model, the dominating factors for the self-heating effects in SNWTs can be investigated which are important for device and circuit thermal-aware design.

2. Electro-thermal Model of GAA SNWTs

This section describes the electro-thermal model based on the equivalent thermal network of SNWTs. Both structure features of SNWTs and thermal conductivity model of silicon nanowire channels are included.

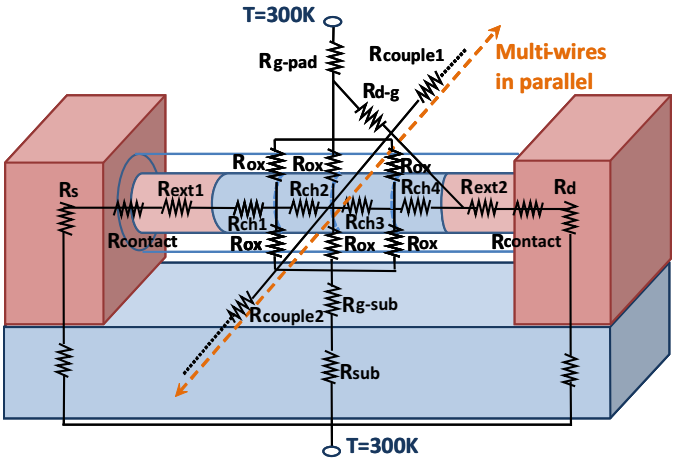

Fig.1 Schematic of a GAA SNWT on bulk substrate with equivalent thermal resistances.

As schematically shown in Fig.1, heat generated in GAA SNWTs can dissipate along the channel towards both source/drain (S/D) region and gate region and ultimately reach the heat sink through pads or silicon substrate. There are also thermal coupling between parallel nanowires through the shared poly-silicon gate region.

The electro-thermal model of GAA SNWTs is combined by an electrical model and a thermal resistance network which couples with each other. Electrons traveling along the channel

interact with phonons and finally generate heat. The generated heat is added to the node in the thermal resistance network, which is the centriod of heat generation profile in the device. Temperature at each node of the network can be obtained through $T=Q\cdot R_{th}+T_0$, where Q is heat, R_{th} is thermal resistance, T_0 is room temperature in this work. The average temperature in the channel is then used back to the current model to adjust the temperature dependent electrical parameters.

An analytic I-V model for GAA SNWTs proposed in our previous works [20] is used as the electrical model in this work. The temperature dependent parameters in the I-V model are

$$\mu = \mu_0 (T_{eff} / T_0)^{\alpha} \tag{2}$$

$$v_{sat} = \frac{v_{sat0}}{(1-\beta)+\beta\cdot(T_{eff}/T_0)} \tag{3}$$

$$SS = SS_0 \cdot T_{eff} / T_0 \tag{4}$$

where α is extracted to be -1.28 for electrons and -0.6 for holes from our experiments. The relation between saturation velocity and temperature is obtained from [21], and β is 0.74 for electrons and 0.34 for holes. T_{eff} is the average temperature in the channel when taking into account the self-heating effects. Other temperature dependent electrical parameters are calculated by replacing T_0 with T_{eff}.

2.1 Modeling of Thermal Conductivity of Silicon Nanowire Channels

Thermal conductivity of silicon nanowires is found to be more than 2 orders of magnitude lower than the bulk value in experiment due to the size effect and high surface to volume ratio [18, 25-26]. In order to accurately simulate self-heating effects, we take into account phonon-boundary scattering and phonon-surface roughness scattering and investigated the combined impact of surface roughness, diameter and length on thermal conductivity of silicon nanowire channels. Effective phonon mean free path can be obtained via Mathiessen's rule. Since thermal conductivity is proportional to phonon mean free path, the effective thermal conductivity of silicon nanowire channels can be given as

$$k_{nw} = \frac{k_b}{1+\dfrac{A}{\dfrac{d}{\lambda_b}-\dfrac{d^2}{4\lambda_b^{\,2}}}+\dfrac{B\Delta^2}{d^2}+\dfrac{C\cdot\lambda_b}{L}} \tag{5}$$

where λ_b is the phonon mean free path for bulk silicon and is 300nm in room-temperature, d is the diameter of silicon nanowires, Δ is the root-mean-square surface roughness height of silicon nanowires, autocovariance length is fixed to 6nm [18] and L is the length of silicon nanowires. A and B are fitting parameters, and C is obtained according to [12].

2.2 Modeling of Thermal Resistances in Equivalent Thermal Network

In the thermal model, thermal resistances should be carefully calculated taking into account of the unique structure features of SNWTs. The thermal conductivity model of silicon nanowire channels is used in thermal resistance calculation. There are three kinds of thermal resistances, which describe the heat flow from plane to parallel plane, the heat flow from nanowire to parallel plane and the heat flow from nanowire to vertical plane respectively.

The traditional thermal resistances of heat dissipating from one plane to parallel plan can be written as $R_{th}=L/(k\cdot A)$, where k is the thermal conductivity of the material in the heat conduction path, L denotes the length of the heat conduction path and A is the cross section area of heat conduction.

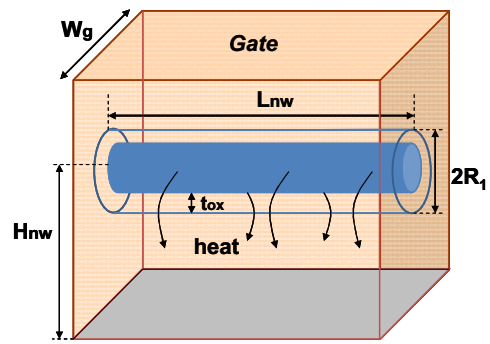

Fig.2 Heat conduction from silicon nanowires to substrate.

As shown in Fig.2, heat flows from silicon nanowire to the substrate via the gate stack. The thermal resistance in this dissipation path is defined as $R_{n\text{-}p}$ and it contains two parts. One is the spreading thermal resistance R_{sp}, representing the heat flow from the silicon nanowire to gate region. The other one is R_m which denotes the heat dissipation towards the substrate as usual. Similar to [22], the spreading thermal resistance for heat dissipation from a small area to a larger area can be given as

$$R_{sp} = \frac{H_{nw}}{k_g W_g L_{nm}} + \left(\frac{1}{\sqrt{2R_1}} - \frac{1}{\sqrt{W_g}}\right)\cdot\frac{\varphi}{k_g\sqrt{\pi L_{nm}}} \tag{6}$$

where

$$\varphi = \frac{\tanh\left(H_{nw}\sqrt{\dfrac{\pi^3}{W_g L_{nm}}}+\dfrac{H_{nw}}{\sqrt{2R_1 L_{nm}}}\right)+\dfrac{k_g}{h}\left(\sqrt{\dfrac{\pi^3}{W_g L_{nm}}}+\dfrac{1}{\sqrt{2R_1 L_{nm}}}\right)}{1+\dfrac{k_g}{h}\left(\sqrt{\dfrac{\pi^3}{W_g L_{nm}}}+\dfrac{1}{\sqrt{2R_1 L_{nm}}}\right)\cdot\tanh\left(H_{nw}\sqrt{\dfrac{\pi^3}{W_g L_{nm}}}+\dfrac{H_{nw}}{\sqrt{2R_1 L_{nm}}}\right)} \tag{7}$$

so the total thermal resistance $R_{n\text{-}p}$ can be obtained

$$R_{n-p} = R_{sp} + \frac{H_{nw}}{k_g \cdot L_{nm} \cdot W_g} \tag{8}$$

where k_g is the thermal conductivity of gate materials; h is the constant heat transfer coefficient, which equals to $1/(R_i \cdot W_g \cdot L_{nm})$, R_i is the substrate thermal resistance.

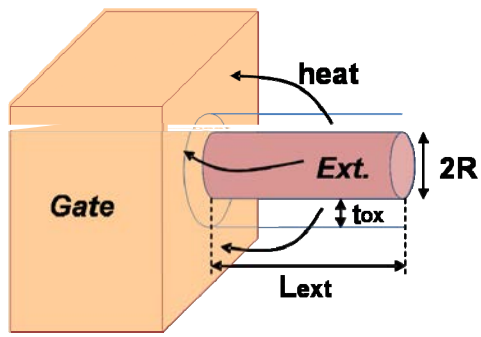

Fig.3 Heat conduction from S/D extension region to gate region.

Fig.3 shows the thermal resistance $R_{d\text{-}g}$ in the heat flows from extension region to the vertical plane of gate region. Similar to outer-fringing capacitance modeling [23-24], $R_{d\text{-}g}$ can be expressed as

$$R_{d-g} = \frac{1}{4k_{ox}\left(L_{ext} - t_{ox} + R\ln(\frac{L_{ext}}{t_{ox}})\right)\cdot\sqrt{\frac{2R}{L_{ext}+2R+t_{ox}}}} + \frac{R_{if}}{2\cdot\pi\cdot R\cdot L_{ext}} \tag{9}$$

where k_{ox} is the thermal conductivity of SiO_2, R_{if} is the total interface thermal resistance of gate stack.

3. Results and Discussions

As shown in Fig.4, the compact thermal conductivity model of silicon nanowires agrees well with both simulation results and experimental results. The figure shows that the thermal conductivity of silicon nanowire channels decrease obviously with the scaling of diameter, especially when the surface roughness is small. When surface roughness decreases, the thermal conductivity of silicon nanowires significantly increases.

Note that, here we discuss the worst case of device self-heating when the devices work in static operation, and the heat generated in the device can be approximately assumed as

$$Q = P = I_{ds} \cdot V_{ds} \tag{10}$$

The whole electro-thermal model is verified by experimental results for both nSNWTs and pSNWTs. Fig.5 and Fig.6 show the results of with self-heating I_d-V_d and I_d-V_g models of twin-nanowire SNWTs. It can be observed from the figure that good agreement between our work and experimental results is obtained.

In order to analyze self-heating effects in GAA SNWTs, we embedded the electro-thermal model in HSPICE simulation. Default device parameters are normalized to their values in Table 1. Fig.7 and Fig.8 show the sensitivity of normalized current driving capability and peak temperature of SNWTs to various device parameters. It can be obtained that the diameter of silicon nanowire channels and the length of S/D extension region are the dominant factors for both the current driving capability and heat dissipation. The height of gate region, the height and the width of S/D region have negligible impacts on self-heating effects in SNWTs. It possibly results from the scaled device dimension which induces the increase of gate thermal resistance. Heat dissipation from channel towards

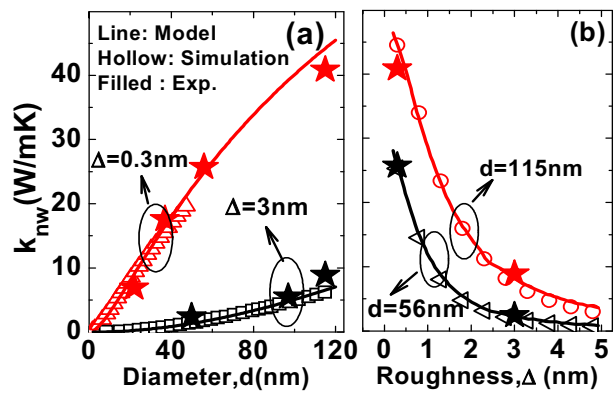

Fig.4 (a), (b) Comparison of silicon nanowire thermal conductivity among our work, simulation results [18], and experimental results [26-27] at very long length.

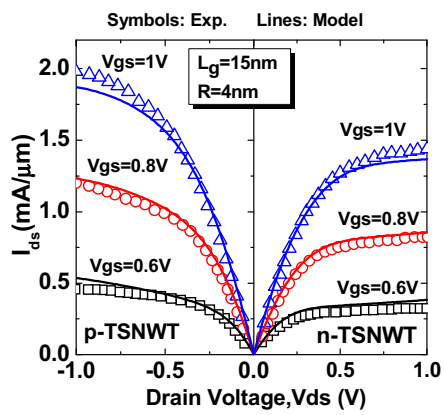

Fig.5 Comparison of I_d-V_d curves between experiment [28] and the proposed model.

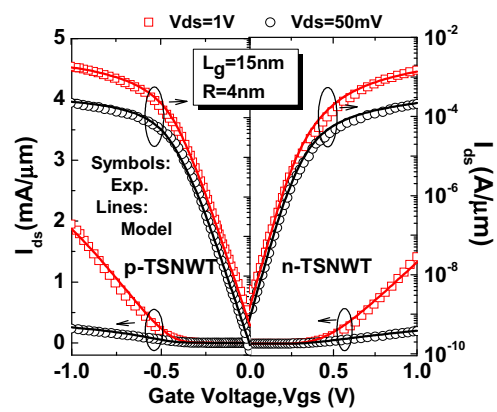

Fig.6 Comparison of I_d-V_g curves between experiment [28] and the proposed model.

Table1. SNWT dimensions and thermal conductivities

Lg	Tox	R	Kpolysi
50nm	3.5nm	5nm	43W/mK (ref[29])
Hg	Hsd	Wsd/Lsd	
400nm	200nm	100nm	Ksi(S/D)
Pitch	Lext	△	62W/mK (ref[29])
40nm	10nm	0.3nm	

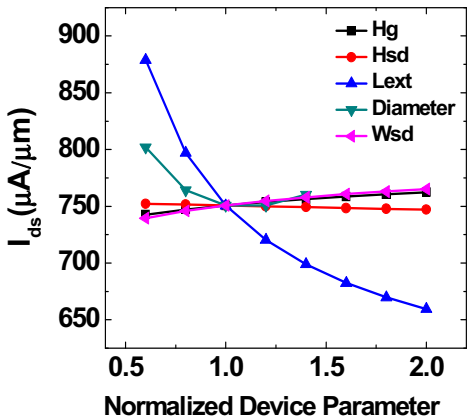

Fig.7 Sensitivity of normalized current driving capability to different device parameters. Device parameters are normalized to their value in Table.1.

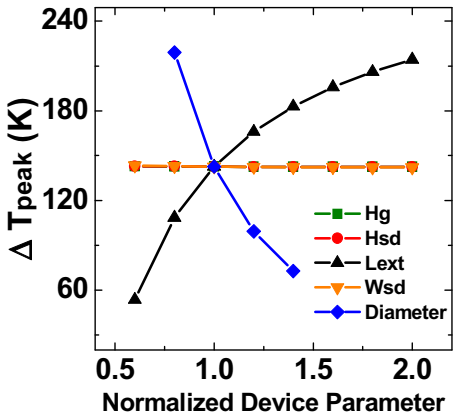

Fig.8 Sensitivity of peak temperature to different device parameters. Device parameters are normalized to their value in Table.1. The total power consumption is kept constant.

gate region is blocked. In this case, heat in the channel may prefer to transport via the silicon nanowires towards S/D region. Therefore, the thermal resistance of silicon nanowire channels is important for self-heating effects in SNWTs. In addition, as discussed above, the reduced thermal conductivity of silicon nanowire channels is sensitive to the diameter of silicon nanowires, and thus the thermal resistance of silicon nanowire channels changes obviously with diameter. On the other hand, it is possible that the generated heat dissipates towards both gate region and S/D region. However, the sensitivity of gate stack thermal resistance to the size of gate region is less significant than that of silicon nanowire thermal resistance to the size of silicon nanowire channels. It can be seen that a shorter S/D extension region is beneficial for suppressing self-heating effects in SNWT, which is helpful for reducing parasitic electrical resistance as well.

4. Conclusion

In this paper, an electro-thermal model for GAA SNWTs, which takes into account the critical features of SNWTs and the impacts of geometry and surface roughness on thermal conductivity of silicon nanowire channels, is accurately developed for the first time to analyze self-heating effects. Good agreements between the model and experimental results are obtained. The sensitivity analysis shows that the diameter of silicon nanowire channels and the length of S/D extension region are the most important factors that influence the self-heating effects in SNWTs. This electro-thermal model is essential for the thermal-aware design of SNWT-based circuits.

Acknowledgements

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